What is claimed is:

1. A programmable motion estimation module for processing pixel values from a sequence of digital images, said programmable motion estimation module comprising:

a programmable microcontroller;

a scalar register file coupled to said programmable microcontroller, said scalar register file comprising a plurality of scalar registers;

a control register file coupled to said programmable microcontroller, said control register file comprising a plurality of control registers;

a crossbar logic unit coupled to the control register file and responsive to one or more control registers of the plurality of control registers;

a direct memory access unit coupled to the control register file and responsive to one or more control registers of the plurality of control registers;

a memory subsystem, responsive to the direct memory access unit, for storing pixel values, said memory subsystem having an image data input for receiving pixel values;

a plurality of processing elements each with plurality of inputs and at least one output coupled to the scalar register file; and

a crossbar switch operable to distribute pixel values stored in the memory subsystem to at least one input of the plurality of inputs of the processing elements, said crossbar switch responsive to the crossbar logic unit.

2. A programmable motion estimation module as in claim 1 wherein a processing element of the plurality of processing elements comprises:

a first input of the plurality of processing element inputs for receiving a first pixel value;

a second input of the plurality of processing element inputs for receiving a second pixel value;

a means for calculating the absolute value of the difference between the first pixel value and the second pixel value; and

an accumulator comprising a register for storing an accumulated value and an adder for adding the accumulated value to the absolute value of the difference between the first pixel value and the second pixel value to obtain a new accumulated value, said accumulator being

coupled to an output of the at least one outputs of the processing element.

3. A programmable motion estimation module as in claim 2, wherein the first and second inputs of the processing element of the plurality of processing element inputs are coupled to the crossbar switch.

4. A programmable motion estimation module as in claim 2, wherein the processing element of the plurality of processing elements further comprises a coupling register for storing said second pixel value.

5. A programmable motion estimation module as in claim 4, wherein the processing element of the plurality of processing elements further comprises a first multiplexer operable to couple said second input of the plurality of processing element inputs to one of the crossbar switch and a coupling register of another processing element.

6. A programmable motion estimation module as in claim 4 wherein the first input of the plurality of processing element inputs is coupled to the crossbar switch and the second input of the plurality of processing element inputs is coupled to the coupling register of another processing element.

7. A programmable motion estimation module as in claim 6, wherein the plurality of processing elements are coupled in series.

8. A programmable motion estimation module as in claim 2 wherein the processing element of the plurality of processing elements further comprises:

a first interpolation element operable to calculate a first interpolated value from a pair of adjacent pixels;

a second interpolation element operable to calculate a second interpolated value from a pair of adjacent pixels;

a third interpolation element operable to calculate a third interpolated value from said first and second interpolated values;

a second multiplexer operable to select said first input of the plurality of processing element inputs to be one of a value from the crossbar switch, the first interpolated value and the third interpolated value.

9. A programmable motion estimation module as in claim 1, wherein said direct memory access unit is operable to generate automatically the addresses of pixel values stored in the memory subsystem in accordance with a programmed access pattern.

10. A programmable motion estimation module as in claim 1, further comprising a system interface element operable to couple the image data input of the memory subsystem and a scalar register of the plurality of scalar registers to a host video processing system.

11. A programmable motion estimation module as in claim 10, further comprising an instruction memory for storing instructions, wherein the system interface element is operable to transfer program instructions from a host video processing system to the instruction memory.

12. A programmable motion estimation module as in claim 1, further comprising

a first arithmetic unit coupled to at least two of the plurality of scalar registers of the scalar register file;

a first conditional flag storage unit for storing flags resulting from the operation of the first arithmetic unit, said first conditional flag storage coupled to said microcontroller.

13. A programmable motion estimation module as in claim 12, further comprising

a second arithmetic unit coupled to at least two of the plurality of control registers of the control register file;

a second conditional flag storage unit for storing flags resulting from the operation of the second arithmetic unit, said second conditional flag storage unit coupled to said microcontroller.

14. A programmable motion estimation module as in claim 13, wherein said microcontroller comprises:

a first memory operable to store program instructions;

a program counter;

a second memory operable to store a program instruction to be performed;

a first instruction decoder; and

a next address logic unit operable to determine the address of a program instruction to be performed, said next address logic unit coupled to the program counter, the first instruction decoder and the first and second conditional flags storage units and responsive thereto.

15. A programmable motion estimation module as in claim 14 configured as a three-stage pipeline, the stages being instruction fetch, instruction decode and execution and write-back.

16. A programmable motion estimation module as in claim 14, wherein the program instructions comprise a 10-bit opcode followed by 22 bits of additional information.

17. A programmable motion estimation module as in claim 14, wherein each of the program instructions is one of a computational instruction, a data transfer instruction, a branch instruction and a special instruction.

18. A programmable motion estimation module as in claim 1, wherein said memory subsystem comprises static random access memory and a virtual memory translation unit.

19. A programmable motion estimation module as in claim 18, wherein said virtual memory translation unit is operable to provide an abstract view of the static random access memory as two-dimensional space indexed by horizontal and vertical coordinates of a pixel.

20. A programmable motion estimation module as in claim 18, wherein said virtual memory translation unit is responsive to one or more control registers of the plurality of control registers in the control register file.

21. A programmable motion estimation module as in claim 18, wherein the static random access memory has at least 3424 entries, each entry being 6-bits.

22. A programmable motion estimation module as in claim 18, wherein the static random access memory is single-ported.

23. A programmable motion estimation module as in claim 18, wherein the static random access memory comprises:

a plurality of search window memory elements operable to store pixel values from a previous digital image;

a plurality of current macroblock memory elements operable to store pixel values from a macroblock within a current digital image; and

a plurality of boundary memory elements operable to store pixel values from a boundary of a previous digital image.

24. A programmable motion estimation module as in claim 1, wherein the crossbar logic unit is operable to process control bitmasks stored in control registers of the plurality of control registers.

25. A programmable motion estimation module as in claim 1, wherein the direct memory access unit is controlled through values stored in by operable to process control bitmasks stored in control registers of the plurality of control registers.

26. A programmable motion estimation module as in claim 25, wherein the direct memory access unit contains a plurality of DMA registers operable to control the functionality of the direct memory access unit, wherein said plurality of DMA registers are memory-mapped to control registers of the plurality of control registers in the control register file.

27. A method for estimating a motion vector relating a macroblock of pixels in a current digital image frame to a macroblock of pixels in a previous digital image frame, said method comprising:

storing a program of instructions in a first memory within a motion estimation module;

transferring pixel data from said previous digital image frame from a host processor to a second memory within said motion estimation module;

transferring pixel data from said current digital image frame from the host processor to the second memory within said motion estimation module;

operating a micro-sequencer to decode said program of instructions sequentially to obtain control signals;

configuring said motion estimation module in accordance with said control signals;

causing said motion estimation module to process the pixel data from said previous and current digital image frames in accordance with said control signals and thereby generate an estimated motion vector; and

transferring said estimated motion vector from said motion estimation module to the host processor.

28. A method as in claim 27, wherein said motion estimation module includes a crossbar switch, wherein an instruction of said program of instructions includes a bitmask and wherein said configuring comprises controlling the functionality of the crossbar switch using said bitmask.

29. A method as in claim 27, wherein said motion estimation module includes a systolic array, wherein an instruction of said program of instructions includes a bitmask and wherein said configuring comprises controlling the functionality of the systolic using said bitmask.

30. A method as in claim 27, wherein said motion estimation module includes a scalar processing element and wherein said configuring comprises controlling the functionality of the a scalar processing element in accordance with an instruction of said program of instructions.

31. A method as in claim 27, wherein said motion estimation module operates as a three-stage pipeline comprising Instruction Fetch (IF), Instruction Decode (ID) and Execution and Write Back (EX) stages.